UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,190	01/20/2006	Masahiro Nomura	Q92733	9238

23373 7590 06/08/2009

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
06/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,190	NOMURA, MASAHIRO	
	Examiner	Art Unit	
	HIEP NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,7,10,11,14,18-26 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,10,11,14,20,21 and 23-26* is/are allowed.

6)☒ Claim(s) *1-3,18,19,22 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "a plurality of stacked inverter stages" in claim 19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 18, 19 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchida (US 5,926,046).

Regarding claim 1, figures 13 and 25 show a multiple-supply-voltage semiconductor device comprising:

at least one first block (223-226) receiving a variable supply voltage (200) , said at least one first block receiving a clock signal; and

at least one variable delay circuit (221, 222) which provides a delay in the clock (CLK) received by the at least one first block, the delay changing wherein in accordance with a change in the supply voltage provided to the at least one first block;

wherein the clock signal (CLK) received by the at least one first block is different from a clock signal received by an at least one second block(121, in figure 25). Note that in circuit (200) of figure 13, the voltage at node between resistor (210) and (211) varies with the supply voltage (Vcc) and circuit (31) adjusts this voltage accordingly.

Regarding claims 18 and 19, the multistage inverter or stacked inverter stage comprises inverters (221, 222).

Regarding claim 2, the at least one variable delay circuit includes circuitry to increase the delay as the supply voltage (Vcc) decreases. Note that the delay of circuit (221, 222) has a delay that is higher when the supply voltage decreases.

Regarding claims 3 and 29, figures 13 and 25 show a multi-supply-voltage semiconductor device comprising:

at least one first block (223-226) receiving a variable supply voltage, said at least one first block receiving a clock signal (CLK);

a voltage level detector circuit (200) which detects a voltage level of the supply voltage (Vcc) ; and

at least one variable delay circuit (221, 222) which provides a delay in the clock signal received by the at least one block, the delay changing wherein the delay changes in accordance with a change in the voltage level detected by the voltage level detector circuit, wherein the clock signal received by the at least one first block is different from a clock signal received by an at least one second block (121, in figure 25). Note that in circuit (200) of figure 13, the voltage at node between resistor (210) and transistor (211) varies with the supply voltage (Vcc) and circuit (31) adjusts this voltage accordingly. The voltage level detector circuit outputs the detected voltage level as a voltage level detect signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US 5,926,046).

Regarding claim 22, figure 13 of Uchida shows a multi-supply-voltage semiconductor device comprising:

at least one block (221) receiving a variable supply voltage, said at least one block receiving a clock signal (CLK);

a voltage level detector circuit (200) which detects a voltage level of the supply voltage; and

at least one variable delay circuit (222-225) which provides a delay in the clock signal received by

the at least one block (221) , said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit. The voltage level detector circuit (200) is not a differential amplifier into which the supply voltage and a reference voltage is input. It is obvious to one of ordinary skill in the art that the complicate level detector (200) of Uchida can be replace with a simpler circuit such as diode or a differential amplifier having a reference input voltage.

Allowable Subject Matter

Claims 6, 7, 10, 11, 14, 20, 21 and 23-26 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIEP NGUYEN whose telephone number is (571)272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donovan D. Lincoln can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan Lam/
Primary Examiner, Art Unit 2816
/Hiep Nguyen/
Examiner, Art Unit 2816
06-04-09